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An undergraduate laboratory experiment for measuring the energy gap in semiconductors

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Abstract. A simple and inexpensive apparatus is described which allows fast and reliable measurements to be made of the temperature dependence of the electrical conductivity in a semiconductor sample. The energy gap can be calculated from the data taken in the intrinsic region, and the temperature dependence of the majority carrier mobility can be deduced from measurements taken in the extrinsic region.

Riassunto. Un apparato semplice e poco costoso permette misure rapide ed accurate della resistenza di un semiconduttore in un ampio intervallo di temperature. Dai dati ottenuti in zona intriseca si calcola l'ampiezza della banda proibita, e da quelli ottenuti in zona estrinseca la dipendenza dalla temperatura della mobilità dei portatori maggioritari.

1. Introduction

In an introductory course on solid state physics semiconductors are frequently characterised by the peculiar temperature behaviour of their electrical conductivity σ. (Two useful texts on this subject are McKelvey (1966) and Smith (1981).) A measurement of σ versus the absolute temperature T, in a sufficiently wide temperature range, may offer a remarkable experimental test of the theoretical predictions of the band model. The apparatus described here does not require expensive instrumentation and allows precise measurements in a relatively short time interval.

We will assume that the student understands the basic ideas of electron–hole pair generation and of electron scattering processes in solids, and therefore we will simply recall here some relationships that are useful in discussing the data collected in the experiment.

The conductivity is defined as the reciprocal of the resistivity $\rho = RA/d$ (where R is the resistance, A the cross section and d the length of the semiconductor sample), or equivalently as the ratio between the current density $J = I/A$ and the applied electric field $E = V/d$, where I is the current measured when the voltage V is applied across the sample ($\sigma = 1/\rho = J/E$).

A doped semiconductor is said to exhibit *extrinsic* behaviour when the dopant concentration N_d is much larger than the concentration of the electron–hole pairs n_i generated by thermal excitations. In this case, provided the temperature is not too low, the 'free charge' concentration $n = n_i + N_d \simeq N_d$ is temperature independent and the charge transfer is essentially due to the majority carriers (holes in p-doped or electrons in n-doped samples). At even lower temperature the semiconductor enters the so called 'freeze-out region' and the impurity carrier concentration decreases exponentially as $\exp(-\varepsilon_d/2K_BT)$, where ε_d is the impurity ionisation energy ($\varepsilon_d \simeq 10$ meV in Ge and $\varepsilon_d \simeq 40$ meV in Si) and K_B is the Boltzmann constant.

In the extrinsic region the current density can be written simply as $J = qnv_D = qn\mu E$, where v_D is the drift velocity, μ the mobility and q the elementary charge. The electrical conductivity is proportional to the charge carrier concentration and to the mobility: $\sigma = qn\mu$. Therefore, in the extrinsic region, since $n \simeq$ constant the temperature dependence of the conductivity and the mobility are identical. Theoretical calculations (see e.g. Shockley (1950), Blakemore (1985)), accounting for lattice scattering of the charge carriers and neglecting contributions due to scattering with impurities, give a mobility

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$\mu \propto T^{-\alpha}$, with $\alpha = 3/2$. The experimentally observed α value, however, is usually larger than the predicted value 3/2, ranging from 1.6 to 2.5.

The thermal generation of the electron–hole pairs grows exponentially with temperature, and when the temperature is high enough the sample enters the *intrinsic* region where N_d becomes negligible with respect to the concentration of thermally generated electrons (n_i) and holes ($p_i = n_i$). In the intrinsic region we must use the ambipolar conduction formula $\sigma = q(n\mu_n + p\mu_p) = (1+b)n_i\mu_n$, where the mobility ratio $b = \mu_n/\mu_p$ is nearly temperature independent (McKelvey 1966, Smith 1981). We have $n_i = p_i \propto T^{3/2}\exp[-E_g(T)/2K_BT]$, where $E_g(T) = E_g(0) - \gamma T$ is the temperature-dependent (Kittel 1968) energy gap that separates the conduction band from the valence band. Here the temperature dependence of the conductivity is largely dominated by the exponential dependence of the carrier concentration, so that a semilogarithmic plot of σ versus $1/T$ yields a straight line with slope $E_g(0)/2K_B$. (The temperature dependence of the energy gap was measured by optical absorption by Macfarlane *et al* (1957, 1958). Above 200 K the results are well described by $E_g = (0.782 - 0.0004T)$ eV for Ge and by $E_g = (1.205 - 0.0003T)$ eV for Si.)

2. Experimental apparatus

The experiment can be performed using a constant current generator, a voltmeter with high input resistance, a thermometer and a device for changing the sample temperature at a small and constant rate (temperature controller).

We found in fact that, for an undergraduate laboratory experiment, it is more practical to take data during a controlled temperature drift than to wait for equilibrium to be reached between two consecutive temperature settings. Fast temperature settings can only be achieved by using a sophisticated automatic thermoregulator, equipped with a feedback-loop gain controlled by both the error signal and its time derivative (Bruschi *et al* 1985). On the other hand the errors in temperature introduced by non-equilibrium conditions can be accounted for in the data handling, as explained below.

In our set-up the temperature controller is made of an oven and a simple electronic driving circuit. The oven is obtained from a metallic cylinder (20 mm diameter copper tube with a closed end) wound with a 50 Ω constantan wire heater. The cylinder is suspended inside a glass dewar (figure 1) by means of a stainless steel thin-walled tube which carries six 0.1 mm diameter copper wires (two for the heater, two for the sample bias current, two for the voltage output) and the thermocouple wires. The steel tube provides an effective thermal decoupling from room temperature. Its upper end is soldered to a holder for electrical connection with the measuring apparatus. When the sample temperature must be lowered below 300 K, a copper braid, soldered to the bottom of the oven, provides a good thermal link to a liquid nitrogen (or dry ice/aceton) bath.

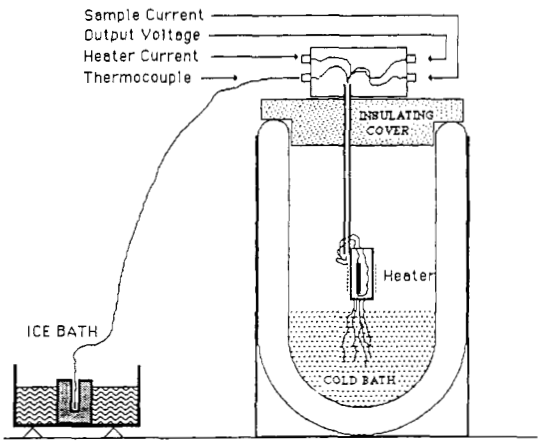

Figure 1. A schematic drawing of the experimental apparatus.

The semiconductor sample is placed inside the oven with the thermocouple junction fastened by PTFE tape. The thermocouple wires should be thin (≃0.15 mm diameter) to reduce the error in temperature due to conductive thermal coupling. The reference junction must be kept at 0 °C (melting-ice bath): it is convenient to glue it inside a small hole drilled in a metal block, placed into the bath. Alternatively an electronic 'ice point' compensation may be obtained using a diode which senses the room temperature†.

The Seebeck voltage signal is read on a digital voltmeter (10 MΩ input resistance, 10 μV sensitivity) and the temperature is calculated from calibration tables within less than 0.5 °C.

The sample temperature is slowly changed, at a selectable rate, by using the circuit of figure 2(*a*). The heater is driven by a transistor whose working point is voltage controlled through a simple ramp generator. This is simply an IC integrator with a constant voltage input V_i stabilised by a Zener diode. The current charging the capacitor C through the resistor R is kept constant by the feedback loop that holds the inverting input of the operational amplifier to a virtual earth.

Therefore the output voltage is

$$V_H = -(1/C)\int_0^t (V_i/R)\,dt = -(V_i/RC)t.$$

† See e.g. Intersil Catalog 5-1 (1986) AD590 Application Note; National Linear Data Book 9-17 (1982) LM134 Application Note.

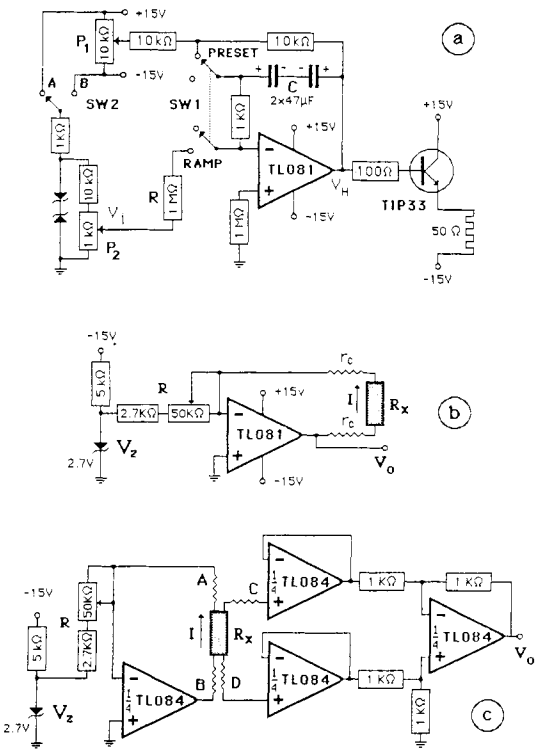

Figure 2. The electronic circuitry: (*a*) heater driver; (*b*) constant-current generator; (*c*) four-wire configuration to avoid the effect of contact resistances.

With the switch SW1 in PRESET, the initial heating power may be chosen through the potentiometer P_1 which sets the voltage across the integrating capacitor C. With the switch SW1 in RAMP, the positive (SW2 in B) or negative (SW2 in A) slope of the ramp generator is chosen by adjusting the potentiometer P_2. Manual control of the heater is possible in the PRESET configuration.

The resistivity of the sample is measured by the simple circuit of figure 2(*b*). Here a constant-current generator provides a selectable and stable current $I = V_z/R$ across the sample. The sample resistance R_x is calculated from the output voltage as $R_x = V_o/I = R(V_o/V_z)$. A typical choice is $R = 2.7\,\text{k}\Omega$, $V_z = 2.7\,\text{V}$ ($I = 1\,\text{mA}$) for samples with R_x up to $10\,\text{k}\Omega$, so that the output reading in volts gives directly the resistance in kΩ. For samples with $R_x < 1\,\text{k}\Omega$, by setting $R = 270\,\Omega$ one can stabilise the current up to 10 mA.

The semiconductor sample is simply a small bar with appropriate electrical contacts. It is important to make the contact resistances r_c negligible with respect to the sample resistance. While it is easy to obtain soldered contacts with low resistance on germanium samples by using regular acid flux and Sn–Pb soft solder alloy, the same procedure on silicon usually gives rectifying and high-resistance contacts (Sconza and Torzo 1985, 1987). Good ohmic contacts can also be obtained on silicon by using 50% Sn–32% Pb–17% Cd–1% Ag eutectic alloy, if an ultrasonic soldering iron is available (we used a model G35/T35 soldering iron and type S-100-a-11 solder, both manufactured by Fibrasonic Inc., Chicago, Illinois). However, we found it more practical to use a unijunction transistor as the silicon sample, taking advantage of the fact that this device has base pins B1 and B2 connected with ohmic contacts to the semiconductor substrate. The emitter pin E, which is connected to the p–n junction, is disregarded for our purposes.

If very low resistance samples are used ($R_x < 100\,\Omega$), the systematic errors due to the voltage drop across the current-carrying wires and to the contact resistances may be not negligible. In this case a four-wire circuit, such as that shown in figure 2(*c*), should be used. Here two separate contact pairs are made at both sample ends: one (AB) for current feed and one (CD) for voltage detection. With this set-up, the potential difference $V_D - V_C$ equals the true voltage drop across the crystal if the measuring instrument sinks a negligible current. The differential amplifier of figure 2(*c*) should be made with FET-input operational amplifiers (input current < 1 nA), or it may be replaced by a high-impedance ($\simeq 100\,\text{M}\Omega$) floating-input voltmeter.

3. The experiment

A typical run is performed in less than 2 h, with the temperature changing at a rate $\partial T/\partial t \simeq 5 \times 10^{-2}\,\text{K s}^{-1}$. Using a liquid nitrogen bath the temperature can be varied in the range $80\,\text{K} < T < 430\,\text{K}$, and with dry ice melting in aceton bath the lower limit is $\simeq 200\,\text{K}$. The upper limit is imposed by the melting of the Sn–Pb solder contacts on the

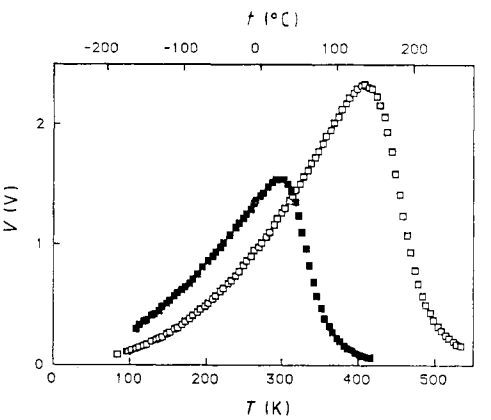

Figure 3. The voltage drop measured across the semiconductor samples in the whole temperature range. The germanium sample (■: $I = 5\,\text{mA}$) is a $2 \times 2 \times 10\,\text{mm}^3$ bar, n-doped. The silicon sample (□: $I = 5\,\text{mA}$) is the base, n-doped, of a 2N2160 unijunction transistor.

germanium sample. If a unijunction transistor is used as sample, one can reach an upper temperature of $T \simeq 520$ K.

It is convenient to use *slightly* doped semiconductor samples, if both the energy gap and the mobility behaviour with temperature have to be measured. The dopant concentration has to be compared with the intrinsic carrier concentration n_i: at room temperature for pure Si we have $n_i \simeq 10^{10}\,\mathrm{cm}^{-3}$ ($\rho \simeq 2.6 \times 10^5\,\Omega$ cm) and for pure Ge $n_i \simeq 10^{13}\,\mathrm{cm}^{-3}$ ($\rho \simeq 43\,\Omega$ cm). In *heavily* doped samples in fact the extrinsic region extends up to high temperatures, and to observe the intrinsic behaviour one has to work above 200 °C where the soft soldered contacts melt. See for example the pressure-contact technique used by Fox and Gaggini (1987)†.

The smaller the temperature slope $\partial T/\partial t$, the smaller are the thermal gradients $\partial T/\partial x$. An evaluation of (and a correction for) the errors due to gradients can be obtained by measuring the resistance at the same observed values of T, both increasing and decreasing the temperature; the average between these two values cancels the systematic error if the slope $|\partial T/\partial t|$ is the same.

The experimental results obtained in two typical runs are shown in figure 3 for a germanium sample (n-doped, $\rho \simeq 14\,\Omega$ cm) and for a unijunction transistor (Texas 2N2160; metal case), respectively. Here T is the temperature in kelvin and t ($= T - 273.15$) is the temperature in degrees celsius.

Figure 4(a) shows the germanium resistance in the intrinsic region plotted versus the reciprocal absolute temperature $1/T$ in a semilogarithmic plot. The slope of the linear fit for $58\,°\mathrm{C} < t < 143\,°\mathrm{C}$ gives $E_g(0) = 0.79 \pm 0.02$ eV. The same plot for the silicon sample is shown in figure 4(b). The best fit in the temperature range $185\,°\mathrm{C} < t < 255\,°\mathrm{C}$ gives $E_g(0) = 1.18 \pm 0.02$ eV.

In figure 4(c), $\log R$ for the germanium sample is plotted versus $\log T$ and the slope of the fitted line for $-160\,°\mathrm{C} < t < -10\,°\mathrm{C}$ gives $\alpha = 1.65 \pm 0.02$. The extrinsic region for the unijunction transistor (figure 4(d)) spans the temperature range $-100\,°\mathrm{C} < t < +100\,°\mathrm{C}$ and the exponent in the power law $\mu \propto T^{-\alpha}$ is $\alpha = 2.30 \pm 0.03$. The slight deviation from linearity at the lowest temperatures indicates the beginning of the 'freeze-out region'.

These results can be compared with the rather scattered α values given in the literature (see e.g. Ziman (1960), Alberigi Quaranta *et al* (1968)) ($\alpha \simeq 1.6$–1.7 for electrons in Ge and $\simeq 2.3$–2.6 for electrons in Si) and with the commonly quoted values (Kittel 1968, Macfarlane *et al* 1957, 1958) for the energy gap linearly extrapolated to 0 K ($E_g(0) = 0.782$ eV in Ge and 1.205 eV in Si). It must be noted here that the measured α value is due to the contribution of various scattering mechanisms. Lattice scattering is dominant in pure and perfect crystals, while impurity scattering and dislocation scattering may become important in less perfect samples. Moreover, α depends on the measuring method, i.e. on conductivity (as in our work), drift time or Hall mobility.

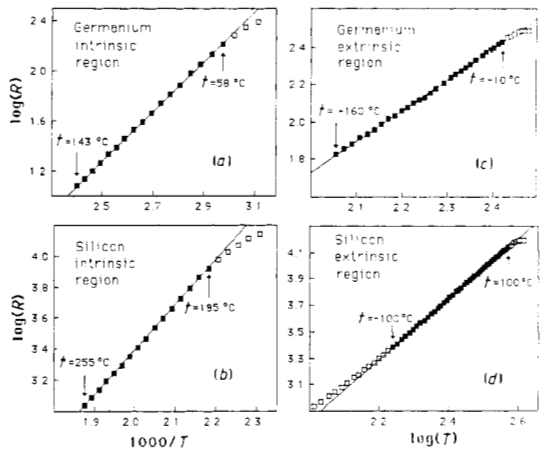

Figure 4. (a) and (b): the linear fit in the intrinsic region (high temperature); (c) and (d): the linear fit in the extrinsic region (low temperature).

† It must be noted that the energy gap of 1.15 eV, quoted by these authors as the expected value for Si, is not the value linearly extrapolated to $T = 0$ K, but the one measured at $T \simeq 0$ K (see Shockley 1950, Blakemore 1985, Kittel 1968, Macfarlane *et al* 1957, 1958).

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